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MULTIPLE POWER DENSITY CHIP STRUCTURE

Abstract

A multiple power density packaging structure with two or more semiconductor chips on a common wiring substrate having a common thermal spreader with a planar surface in thermal contact with the non-active surfaces of the chips. The semiconductor chips have different cooling requirements and some of the chips are thinned to insure that the chips requiring the lowest thermal resistance has the thinnest layer of a thermal adhesive or metal or solder interface between the chip and thermal spreader.